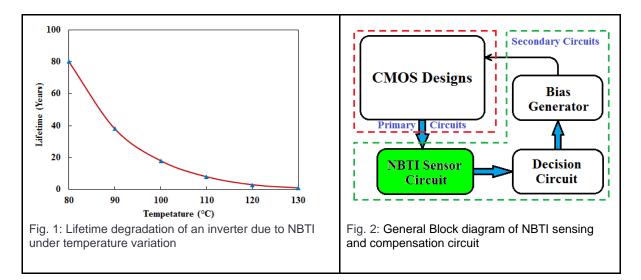
NBTI Analysis and Mitigation Technique in IG-FinFET SRAM Cell

Keywords: NBTI, Reliability, SRAM, Process variation

Write-up:

With continuous scaling of MOSFET technology, the feature size of integrated circuits face many physical limitations. The excessive leakage current and device/circuit reliability are the two major issues in the scaled devices. Transistors suffer from multiple temporal degradations such as Bias temperature instability (BTI), Hot carrier injection (HCI) etc. which may lead to significant discrepancies in the devices. BTI is a time dependent and is caused due to dangling bond defects at Si/SiO₂ interface that allows trapping of charges even at small energy into Si/SiO₂ interface which increases the threshold voltage and affects both the NMOS and PMOS devices [1]. Negative bias temperature instability (NBTI) leads to significant shifts in the threshold voltage of PMOS over a time which creates uncertainty in device/circuit behaviour and decreases the lifetime of the device/circuit. Fig. 1 shows that the lifetime of an inverter is degraded due to NBTI by 2.2 for every 10°C increase in temperature, which means the lifetime of any circuit depends on the operating temperature [2]. Because of this progressive degradation, it is difficult to ensure the reliability of integrated circuit over their lifetime, hence it is essential to explore variation tolerant design solutions to mitigate variability issues.

My research development is to mitigate the threshold voltage shift of transistors in SRAM cell. The complete structure of my development has three steps as shown in Fig. 2. In first step, design the NBTI sensor circuit which sense the change in leakage current due to NBTI. Second step is to compare the stressed value and to generate the different voltages which depends on the amount of threshold voltage shift due to temporal degradation. Third step is to apply those voltages to the body terminal of transistors which performs the opposite effect and to maintain the threshold voltage of transistor hence increase the lifetime.



References

[1] G. D. Panagopoulos and K. Roy, "A three-dimensional physical model for Vth variations considering the combined effect of NBTI and RDF," IEEE Transactions on Electron Devices, vol. 58, no. 8, pp. 2337–2346, 2011

[2] R. Habchi, C. Salame, A. Khoury, and P. Mialhe, "Temperature dependence of a silicon power device switching parameters," Applied Physics Letters, vol. 88, no. 15, p. 153503, 2006.