Ultra High Frequency (UHF) operated Noise Tolerant, Low Power and Highly Stable SRAM Memory System Design for Battery Operated Internet of Things (IoT) Applications

The present internet of things (IoT) enabled processors are operating at GHz frequency range, and the critical register files which occupy a major portion of the complete processor's core area also typically operates at the same speed. Also, with the nano technology nodes the design of low power and energy efficient SRAM subsystem has become a necessity as it is the largest component (70%) of today's system on chip (SoCs) VLSI circuits. Hence, SRAM is one of the most vulnerable components to the effects of power variations. The increasing frequency values of processors push the exponential increment in active power component of memory systems and reaches up to 37% of the total microprocessor's power. A wide worded memory register consumes nearly a quarter value of a watt in 7-10 GHz frequency range, which make them thermally unstable. At lower feature sizes of advanced technology nodes, the flicker noise also gets increased, and would be problematic once smaller feature sizes are employed in memory design. Therefore, as the SRAM is already struggling with the increasing instability, access power (leakage and active both) consumption and and process voltage temperature (PVT) intolerance at ultra low supply voltages in moderns battery operated SoCs, the high frequency processors further putting a major challenge to the SRAM design.

It is proposed to design a SRAM memory system which would be suitable to be used for high frequency processors required in IoT based applications. The striking features of the memory which would be focussed at ultra low supply voltage would be.

1. Increased noise stability for all the operating modes (read/write/standby)
2. Ultra low power consumption
3. High frequency operation of SRAM memory
4. Lower sensitivity to PVT variations and thermal/flicker noise

References:

1. K. Sarfaraz and M. Chan, "A 1.2 V to 0.4V 3.2 GHz to 14.3 MHz Power Efficient 3-Port Register File in 65 nm CMOS", *IEEE Transactions on Circuits and Systems-I: Regular Papers,* vol. 64, No. 2, Feb. 2017.
2. S. Junsangsri, F. Lombardi and J. Han, "Evaluating the Impact of Spike and Flicker Noise in Phase Change Memories", *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, Oct. 2015, USA.
3. J. Samandari and r. Hughey, "Power/Energy Minimization Techniques for Variability-Aware High Performance 16-nm 6T-SRAM", *IEEE Access*, vol. 4, Jan. 2016.